International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

FPGA Implementation of Low Power Multi Serials to Ethernet Gateway for Data Acquisition System

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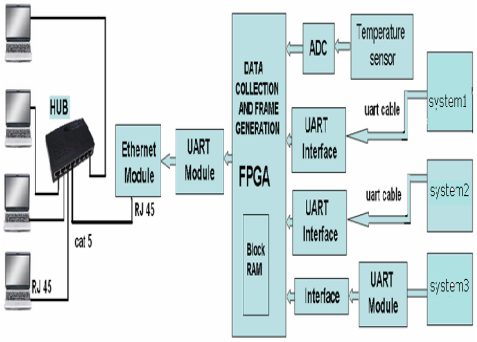
***Abstract* – Data acquisition is the process of sampling signals that measure real world physical conditions and converting the resulting samples into digital numeric values that can be manipulated by a computer. The communication between them is standard asynchronous serial form by typical serial control card, which have complicated cable wiring, frequently interruption of CPU, which greatly reduces the CPU's efficiency and impacts the system's real-time processing. To resolve these problems, a method of multi-serials to Ethernet Gateway based on the field programmable gate array (FPGA) with network interface chip is implemented in this project. The Gateway will send data as Ethernet frame format after receiving serial data, indirectly achieves multi-serials communication, simplifies cabinet wiring and improves CPU's efficiency. In this project we use WIZ net W5100 Hardwired TCP/IP Embedded Ethernet Controller chip will be interfaced to FPGA to provide Ethernet interface. Various digital signals will be captured by FPGA and will be sent on a serial line. The FPGA implements all the necessary logic to read the data from these sensors and store the data in it. On FPGA logic also will be implemented to read data from multiple numbers of serial ports. The WIZ Net module takes data from serial port and sends to PC in Ethernet form. In PC application will be developed to read data from Ethernet and store it on PC hard disk. The code will be developed in VHDL. Modelsim Xilinx Edition (MXE) will be used for simulation and functional verification. Xilinx tools will be used for synthesizing the core to Spartan-3 FPGA. Chip scope will be used for on chip verification of the results.**

***Keywords* – Ethernet, FPGA, Multiserials, Gateway, UART.**

I. INTRODUCTION

The data link is composed of ground control station and data terminal. The computers on the ground need control and check more than ten assemblies, containing main and sub remote control transmitters, telemetry receivers, image decompression board, ground positioning receiver and radio location tracking servo system etc. The communication between them is standard asynchronous serial form and at the current, the serial ports are expanded by MOXA card, whose weaknesses are: complicated cable wiring, frequently interruption of CPU, which greatly reduces the CPU's efficiency and impacts the system's real time processing. To resolve these problems, a method of multiserials to Ethernet Gateway based on the field programmable gate array (FPGA) +network interface chip is presented. The Gateway will send data as Ethernet frame format after receiving serial data, indirectly achieves multi-serials communication, simplifies cabinet wiring and improves CPU's efficiency.

II. BLOCK DIAGRAM



The Gateway mainly consists of FPGA, Ethernet module and level converter. Using a flexible FPGA programming feature, a UART [2] can be designed in it. If several UARTs are in it, the system has the capacity of communication with multiple serial ports. The Ethernet module implements Ethernet communication and is configured at the time of initialization. As we can see in Fig.1, the Gateway's main function is to achieve communication between the serial devices and Ethernet. When it receives data from devices, Gateway will choose useful data from serial data frame following the communication protocol, and send data after packaged. When it receives data from Ethernet, it firstly unpacks the frame and determines the port number to transfer data to its buffer and adds the synchronous heads.

Data acquisition:

Data acquisition is the process of sampling signals that measure real world physical signals that measure real world physical conditions and converting the resulting samples into digital numeric values that can be manipulated by a computer. Data acquisition systems (abbreviated with the acronym DAS or DAQ) typically convert analog waveforms into digital values for processing. The components of data acquisition systems include:

- Sensors that convert physical parameters to electrical signals.
- Signal conditioning circuitry to convert sensor signals into a form that can be converted to digital values.
- Analog-to-digital converters, which convert conditioned sensor signals to digital values.

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Signals/Sensors:

A sensor (or transducer) is a device that converts a physical phenomenon into a measurable electrical signal, such as voltage or current. The following table shows a short list of some common phenomena and the transducers used to measure them.

Transducers convert physical phenomena into measurable signals, however, different signals need to be measured in different ways. For this reason, it is important to understand the different types of signals and their corresponding attributes. Signals can be categorized into two groups: analog and digital.

DAQ Hardware:

Data acquisition hardware acts as the interface between a computer and signals from the outside world. It primarily functions as a device that digitizes incoming analog signals so that the computer can interpret them.

Connection to Signals:

Data acquisitions devices typically consist of one or more of the following functions for measuring different types of signals:

- Analog inputs – measure analog signals
- Analog outputs – generate analog signals
- Digital inputs/outputs – measure and generate digital signals
- Counter/timers – count events or generate pulses

Multifunction data acquisition boards combine analog, digital, and counter operations on a single device. Additionally, some data acquisition boards include integrated signal conditioning specific to a signal or sensor type.

Connection to Computer:

Data acquisition hardware is offered on several different PC busses. Each bus offers different levels of ease-of-use and performance and are better suited for different applications.

Existing System:

Serial expansion cards are used for interfacing with different types of sensors. Separate microprocessor/ microcontroller is used for Ethernet connectivity. Increases the cost, space and power consumption.

Proposed System:

FPGA based multi serial gateway Ethernet connectivity is achieved with small Ethernet adapter (serial to Ethernet). Any other interface can be built on FPGA easily.

III. DATA SENDING MODULE

ADC module:

FPGAs are well suited for serial Analog to Digital (A/D) converters. This is mainly because serial interface consumes less communication lines, while the FPGA is fast enough to accommodate the high speed serial data. The ADCS7476MSPS is a high speed, low power, 12-bit A/D converter. A/D converter is a high speed serial interface that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA.

UART block:

The UART is a serial interface with a frame format of start bit of active low ‘0’at beginning of frame and 8 bit of information with a stop bit of active high‘1’ signal at the end. The operation of UART is controlled by Clock signal which is fed from external crystal.

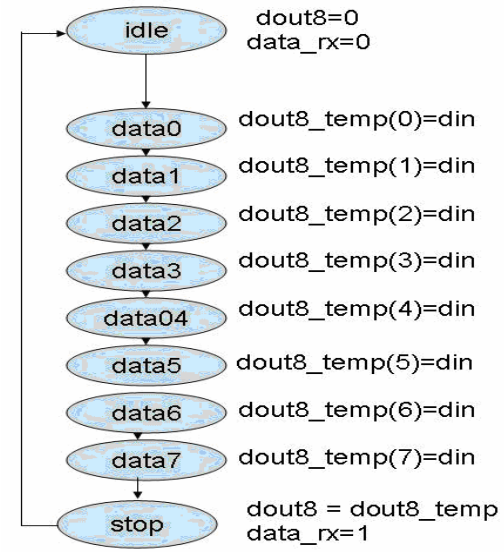
Baud Generator:

Baud generation section is a clock divider circuit, FPGA board clock runs at 50MHz, but UART transfers data at predefined standards that had to be maintained, in present system is designed for a rate of 9600 bits/sec(i.e $50x10^6$ is scaled down for 9600). It generates 9600 pluses per sec; this implies the speed of UART is 9600 bits per sec. Another clock is with a 16 times faster than required, and it is given to the receiver section, so that the data will not be corrupted.

Receiver Section:

UART receiver handles reception of data from RS232 port. Main functions of receiver block are to convert the serial data to parallel data, and check the correctness of data from parity and store the received data. UART receiver state machine is shown in Figure .2.7. The receiver is in IDLE state by default. When the serial data pin goes low, indicating the start bit, the state machine enters DATA0 state. The data is received; one bit at a time from LSB to MSB in states DATA0 to DATA7.

UART receiver state machine:



IV. DATA COLLECTION MODULE

Adc_in, UART ‘s input1,input2 and input3 are the inputs for this block these input’s are selected with select lines that are generated from input address counter Rd_address, wr_address, data, clk and wr_rd are inputs to connection memory module and q is the output.

Data collection process:

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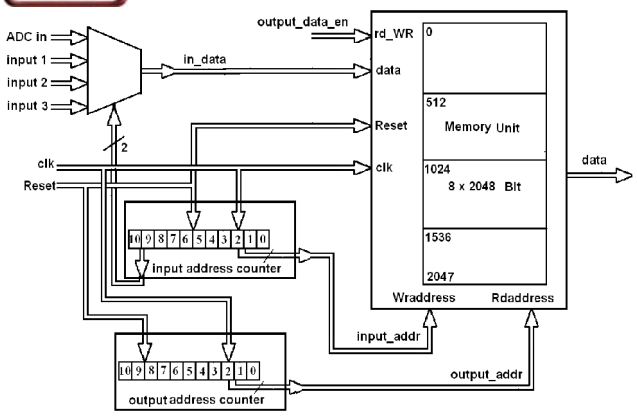
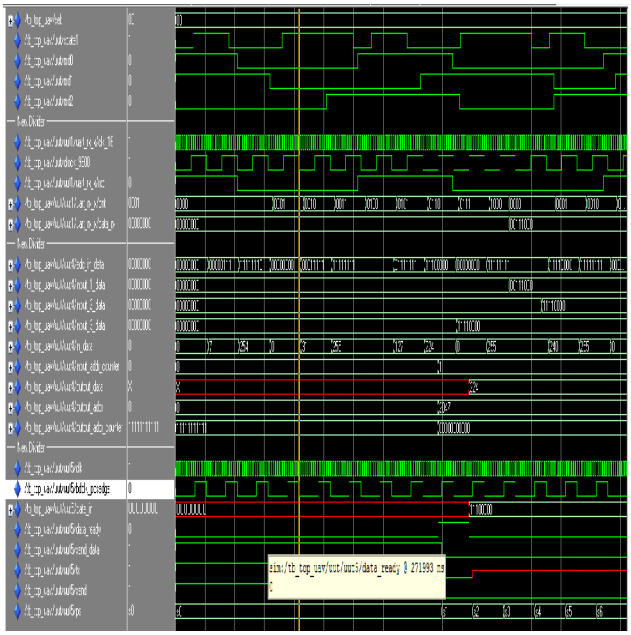


Ethernet module:

The Ethernet module takes the input from the transmitter assigned port of the FPGA in a serial format form, and that data is transmitted to the destination system in the form of Ethernet packet .By Team Tera Pro software we observed the transmitted data in the output PC.

V. Simulation and Results

The results of test denote that the method adopted in this can achieve the original purpose. Using this method, we simplify the communication between monitor computer and port devices, improve the efficiency of CPU, and ensure the processing of system in real time. FPGA's flexible programming features also allow further upgrade for system. This design could be used in the domain of net control and information management system. It has a certain value for application.The simulation results are shown in the below figure:



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